

C routine counts high bits

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A simple C routine counts the number of 1s in a 16-bit word. You can apply the general technique to a word of any length, but for purposes of explanation, assume a word length of 8 bits (Listing 1). If you AND the original word with 01010101 binary, the 8-bit result consists of four 2-bit words. Each of these 2-bit words contains the count of the number of 1s in the least significant bit of the original word's corresponding 2-bit field. Now, shift the word right by 1 bit and again AND the word with 01010101 binary. The resultant group of 2-bit words now contains the count of the number of 1s in the most significant bit of the corresponding 2-bit field in the original word. Adding the results of these two AND operations produces four 2-bit words that each contain the count of the number of 1s in the corresponding 2-bit field of the original word.

Now, use this sum and repeat the above process, except AND the sum with 00110011 binary and shift by two instead of one. The result is an 8-bit sum of two 4-bit words, where each 4-bit word contains the count of the number of 1s in the corresponding 4-bit field in the original word. Use this second sum and repeat the process, except AND with 00001111 binary and shift by four instead of two. The final result, the third 8-bit sum, contains the count of the number of 1s in the entire 8-bit original word.

The assembly code for a TMS320C50 DSP (Texas Instruments, Dallas) counts the number of 1s in a 16-bit word, assuming that the original 16-bit word is in the ACC accumulator at the start (Listing 2). The code stores the final

LISTING 1—C ROUTINE FOR COUNTING 1s

```
int
CountOnes (int word)
{
    int count;

    count = (word & 0x5555) + ((word >> 1) & 0x5555);
    count = (count & 0x3333) + ((count >> 2) & 0x3333);
    count = (count & 0x0F0F) + ((count >> 4) & 0x0F0F);
    count = (count & 0x00FF) + ((count >> 8) & 0x00FF);

    return (count);
}
```

count back in the ACC accumulator. This code requires two clock cycles per bit, or 32 clock cycles to count the number of 1s in a 16-bit word.

The assembly code for the ADSP-2106x SHARC DSP (Analog Devices, Norwood, MA) counts the number of 1s in a 32-bit word, assuming that the original 32-bit word is in R2 at the start (Listing 3). The code stores the result back in R2 at the end. This code requires 25 clock cycles to count the number of 1s in a 32-bit word, which is about 0.78 clock cycles per bit.

The software listings are available for downloading from EDN's Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2132. (DI #2132)

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LISTING 2—TMS320C50 CODE FOR COUNTING 1s

```

SACB          ;1 ACCB = ACC
BSAR 1        ;1 ACC = ACC >> 1
AND #05555h;SHFT ;2 ACC = ACC & 0x5555
EXAR          ;1 ACC <-> ACCB
AND #05555h;SHFT ;2 ACC = ACC & 0x5555
ADDB          ;1 ACC = ACC + ACCB

;
SACB          ;1 ACCB = ACC
BSAR 2        ;1 ACC = ACC >> 2
AND #03333h;SHFT ;2 ACC = ACC & 0x3333
EXAR          ;1 ACC <-> ACCB
AND #03333h;SHFT ;2 ACC = ACC & 0x3333
ADDB          ;1 ACC = ACC + ACCB

;
SACB          ;1 ACCB = ACC
BSAR 4        ;1 ACC = ACC >> 4
AND #0F0Fh;SHFT ;2 ACC = ACC & 0x0F0F
EXAR          ;1 ACC <-> ACCB
AND #0F0Fh;SHFT ;2 ACC = ACC & 0x0F0F
ADDB          ;1 ACC = ACC + ACCB

;
SACB          ;1 ACCB = ACC
BSAR 8        ;1 ACC = ACC >> 8
AND #00FFh;SHFT ;2 ACC = ACC & 0x00FF
EXAR          ;1 ACC <-> ACCB
AND #00FFh;SHFT ;2 ACC = ACC & 0x00FF
ADDB          ;1 ACC = ACC + ACCB
```

LISTING 3—ADSP-2106X CODE FOR COUNTING 1s

```

R3 = 0x55555555;
R4 = LSHIFT R2 BY -1; /* R4 = R2 >> 1 */
R4 = R4 AND R3;
R2 = R2 AND R3;
R2 = R2 + R4;

R3 = 0x33333333;
R4 = LSHIFT R2 BY -2; /* R4 = R2 >> 2 */
R4 = R4 AND R3;
R2 = R2 AND R3;
R2 = R2 + R4;

R3 = 0x0F0F0F0F;
R4 = LSHIFT R2 BY -4; /* R4 = R2 >> 4 */
R4 = R4 AND R3;
R2 = R2 AND R3;
R2 = R2 + R4;

R3 = 0x00FF00FF;
R4 = LSHIFT R2 BY -8; /* R4 = R2 >> 8 */
R4 = R4 AND R3;
R2 = R2 AND R3;
R2 = R2 + R4;

R3 = 0x0000FFFF;
R4 = LSHIFT R2 BY -16; /* R4 = R2 >> 16 */
R4 = R4 AND R3;
R2 = R2 AND R3;
R2 = R2 + R4;
```

Slow op amp makes fast multivibrator

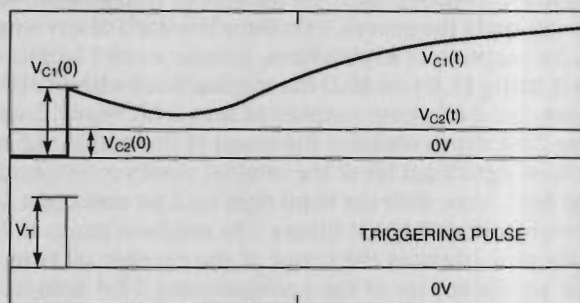
LUKASZ SLIWczynski, UNIVERSITY OF MINING AND METALLURGY, KRAKOW, POLAND

A classic one-shot multivibrator using an op amp (Figure 1a) needs a relatively long-duration triggering pulse, even though the circuit is in theory a slope-triggered configuration. This limitation can be a problem when you want to use a "spare" op amp from a dual or quad package (LM324, LM358, LM6482, or LT1013, for example) triggered from fast logic circuitry. The op amp's limited slew rate (SR) creates the problem. A duration in the order of $t = V_{LH}/SR$ is necessary for the positive-feedback loop through R_1 and R_2 to capture the output in the high state. (V_{LH} is the op amp's output swing.) This value of t is an approximation, because the exact value depends on the amplitude of the triggering pulse, its shape, and the form of the op amp's output transition. A simple modification (Figure 1b) of the basic circuit allows you to trigger the one-shot with a narrow pulse; for example, 5 nsec.

The method uses the nonlinear properties and speed of a basic emitter follower. When the triggering pulse appears, Q_1 turns on and the low-value capacitor, C_1 , rapidly charges to the voltage level $V_{C1} = V_T - V_{BE}$, where V_T is the amplitude of the triggering pulse and V_{BE} is Q_1 's base-emitter voltage, approximately 0.7V. When the triggering pulse ends, Q_1 turns off and C_1 slowly discharges through R_1 and simultaneously charges through R_2 from the linearly increasing voltage from the op amp's output. The circuit acts as a simple pulse stretcher, giving some extra time for the other, slower parts of the circuit. Q_1 replaces diode D_1 in Figure 1a's basic circuit to separate the trigger source from the loading effects of capacitor C_1 . The one-shot's pulse width is

$$T = R_3 \parallel R_4 C_2 \ln \frac{V_O^+ - V_{TH}}{V_O^+ - V_G}, \quad (1)$$

FIGURE 2



The voltage on C_2 in Figure 1b remains relatively constant during the triggering phase; the higher voltage on C_1 keeps the op amp in its high state.

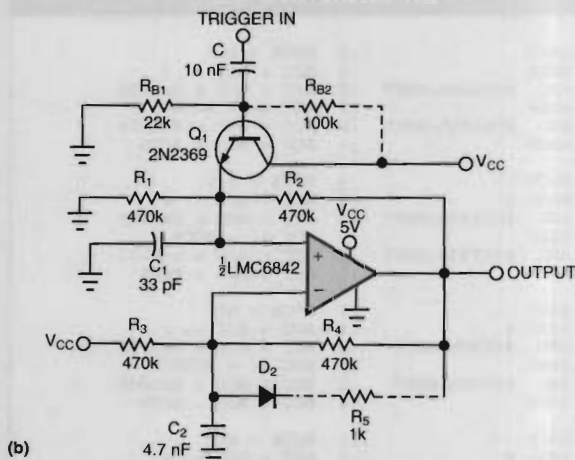
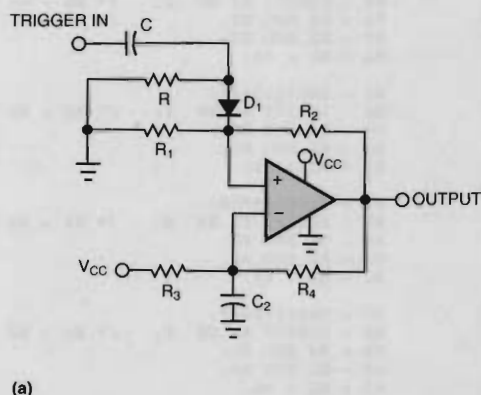
$$V_{TH} \approx V_{BE} + V_O^- \text{ AND } V_G = V_O^+ \frac{R_1}{R_1 + R_2}, \quad (2)$$

provided that

$$V_{TH} > V_O^- \frac{R_1}{R_1 + R_2}. \quad (3)$$

Failing the condition of Equation 2, the circuit forms a free-running oscillator with an approximate 50% duty cycle. The low-value resistor R_5 may be necessary to ensure that C_1 discharges faster than C_2 when the $R_1 \parallel R_2 C_1$ time constant is

FIGURE 1



Replacing a diode (a) with a transistor (b) allows you to use a slow op amp to configure a one-shot multivibrator that works with narrow triggering pulses.

higher than $R_3 || r_D C_2$, where r_D is the dynamic resistance of D_2 . Figure 2 shows the triggering waveforms. $V_{C1(t)}$ and $V_{C2(t)}$ are the voltages on C_1 and C_2 , respectively. Calculating the precise value of C_1 entails solving some complicated nonlinear equations. It's much easier to test the circuit empirically with various capacitor values. The circuit in Figure 1b generates a pulse of approximately 700- μ sec width with a 5-

nsec, 2V triggering pulse. You can lower the triggering-pulse amplitude by approximately 0.7V by using optional resistor R_{B1} to forward-bias Q_1 's base-emitter voltage. (DI #2141)

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Spice 3 models pressure sensors

DEBRA HORVITZ, GALAHAD SYSTEMS, LAGUNA HILLS, CA

Commercially available versions of Spice 3, such as IsSpice4 (Intusoft, San Pedro, CA), can simulate mixed-domain systems containing electrical, mechanical, physical, and mathematical elements using behavioral models. You can use these features to simulate a variety of components. For example, the generic subcircuit in Figure 1 and the corresponding listing model the simple linear behavior of a pressure transducer. Behavioral sources B1 and B2 set up the output-voltage equation. The .SUBCKT call line passes the sensitivity (SENS) and zero-pressure offset-voltage parameters (VOS) into the subcircuit. Spice automatically evaluates each parameter during each simulation.

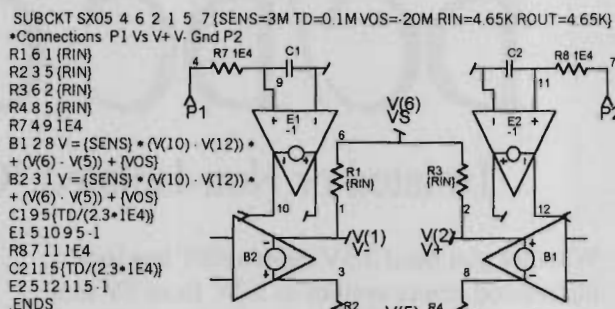
The pressure—in this case, P1–P2—is an input to the subcircuit, as is the supply voltage $V(6)$ – $V(5)$. The resistance RIN models the resistive bridge between the supply voltage and load. The sensitivity units are V/V/psi, but you can alter these units as long as you maintain a consistent set throughout the subcircuit and if you correctly specify the input voltage—which is the analog of pressure. The model gives the correct response time through the use of the R7, C1, and E1 group of delay elements and the R8, C2, and E2 group.

All the generic parameters you need for the model are available from a typical data sheet. For example, the SXO1 pressure sensor (SenSym Inc, Milpitas, CA) has the following typical characteristics at 25°C: sensitivity=4 mV/V/psi, zero pressure VOS=20 mV, input resistance=4.65 k Ω , and output resistance=4.65 k Ω . Thus, a typical call line to the generic model is

```
X1 1 2 3 4 DUCER {SENS=4E-3 VOS=-20E-3
RIN=4.65K ROUT=4.65K} .
```

You can use this subcircuit to model differential, gauge, and absolute sensor devices. Differential devices measure one pressure with respect to another. P1 is typically the high-pressure input and P2, the low. For the differential transducer model in Figure 1, P1 should always remain greater

FIGURE 1



Behavioral-modeling features of Spice 3 allow you to implement a subcircuit model of a pressure sensor. B1 and B2 are behavioral sources that model the transducer's transfer function.

than P2. Gauge devices measure pressure with respect to an ambient pressure. In this case, pressure is measured at one input while the other is set at a desired reference pressure. Absolute devices measure pressure with respect to an internally isolated vacuum chamber. To model these devices, you need to remove the P2 pressure terminal and replace it internally with a dc voltage source of 0.0005V, which represents 0.0005 psia. You have to adjust this number if you use different units.

You generally operate a pressure sensor in a specific pressure range, so this subcircuit models only the linear behavior of a given device. The model does not include nonlinearities associated with the pressure-to-voltage conversion, hysteresis, repeatability, and stability. The model does not include temperature dependencies, but they are easy to add. Also note that there is no limit to the applied pressure. If the applied pressure exceeds the maximum-over-pressure rating, the transducer model operates as if it were a legal condition. (DI #2134)

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Fax saver cuts wear, tear, and power

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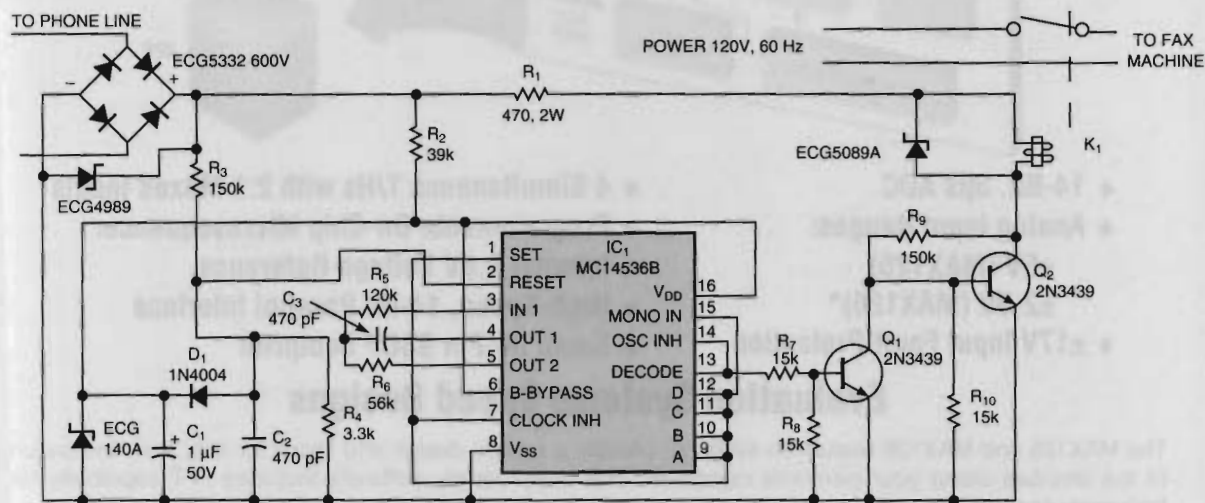
You can build the circuit in **Figure 1** for less than \$20 to cut wear and tear on your fax machine while saving power. If your fax machine has a dedicated phone line, the circuit intercepts the incoming ring signal and powers up the fax machine in time to receive the fax. It then turns off the fax machine after a predetermined time and awaits the next incoming fax. A relay in the line-cord circuit of the machine provides the turn-on and -off functions. If you build the fax saver in a small, plastic, outlet-type box, you can plug the fax machine into the box and wire the phone line in parallel with the machine's phone line.

The circuit incorporates protection against phone-line transients and draws its power from the normal 48V dc on the phone line; you thus need to exercise care in relay selection. Suitable relays are available at low cost from major distributors. The circuit function centers on a long-countdown device, IC₁, whose overall delay depends on the external passive components. Q₁ and Q₂ require a high V_{CE} rating to accommodate transients that can appear on the incoming phone line. (DI #2142)

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FIGURE 1



Put your fax machine to sleep with this easy-to-build circuit that saves wear and tear as well as power.

Battery charger takes on two roles

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The NiCd and NiMH battery charger in **Figure 1** applies a battery fast-charge controller IC in a way that not only provides peak-voltage fast-charge termination—as the IC was designed to do—but also precisely regulates the charge current. The design also features maximum-temperature back-up shutdown. Efficiency exceeds 90% at a V_{IN} of 14V.

The voltage-to-current switching-regulator loop includes a duty-cycle modulator formed by the voltage ramp across the inductor's current-sense resistor, R_S, and a hysteresis

comparator normally used for thermistor-sensed cold-temperature detection. The IC develops the comparator threshold of 100 mV across a 10-kΩ thermistor, which conducts the 30-μA reference that the controller IC provides. R_S creates a level-shifted ramp voltage at Pin 5. When the comparator threshold crosses 100 mV, this ramp voltage causes the comparator to switch off the MTP2955E using an active-low output at Pin 3. The inductor current decreases linearly during the MOSFET off-time until the comparator hysteresis

exceeds 48 mV. As the design equations in Figure 1 indicate, the proper choice of L_1 and R_3 sets the charging current and switching frequency for a particular charger input and output voltage.

In addition to performing duty-cycle-controlled current regulation, the controller IC momentarily interrupts the charging current to perform the A/D conversion. Pin 2 is active-low for 33 msec every 1.4 sec. The first 11 msec are necessary for the battery voltage to settle; the controller IC uses the remaining 22 msec to count VFC pulses for an A/D conversion. By interrupting the charging current, the controller eliminates offsets due to charge-current flow through the charger output cable and through the battery's internal impedance during the battery-voltage sampling measurement. This interruption also eliminates noise induced in the wiring from the switching magnetic fields. The elimination of these error sources, along with the iterating nature of the converter, allows a peak-voltage-detector threshold of only -4 mV for the voltage at Pin 1. This input is a one-cell equivalent voltage developed by the one-fifth voltage divider of R_3 and R_4 .

The threshold of the overtemperature-protection comparator is equal to the voltage at Pin 7. This voltage is equal to the 30- μ A current source flowing from this pin times the value of R_6 . R_6 should be equal to the parallel combination

of R_7 and the value of the thermistor at the upper temperature limit. Because the thermistor voltage sets both the temperature and the current regulation threshold, the design uses R_7 to reduce the temperature sensitivity of the charging current to approximately 30% from 25 to 45°C for a typical thermistor. You can use a lower value for R_7 if this variation is unacceptable, or you can eliminate the thermistor if backup protection is unnecessary.

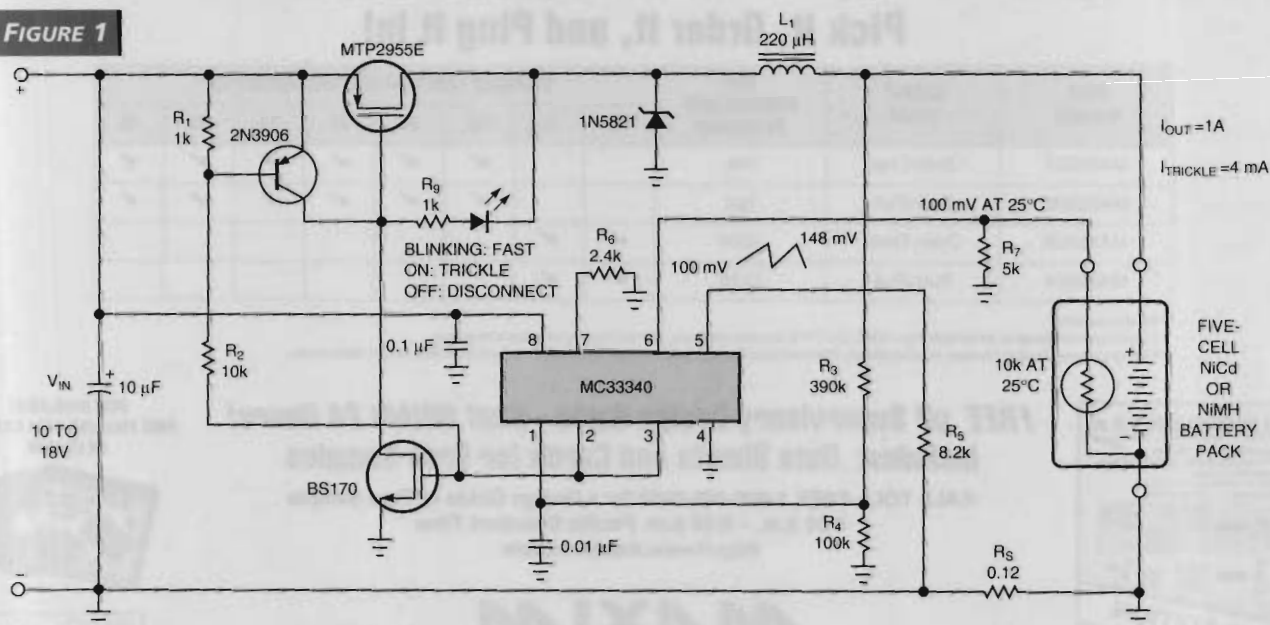
The design includes an LED to indicate charge status. Blinking indicates regulated current fast charge; continuously on indicates fast charge has terminated or the battery pack is undervoltage (less than 1V/cell) or overvoltage (greater than 2V/cell), and continuously off indicates a disconnected input. During the state that fast charging is interrupted, a trickle current equal to $(V_{IN} - V_{LED} - V_{OUT})/R_9$ flows into the battery.

A lower cost alternative is to replace the MTP2955E with a TIP42 pnp power transistor and replace the BS170 with a 1-k Ω resistor to ground. This approach reduces efficiency by 5 to 10% because of the slower switching of the pnp transistor as well as the power dissipated in the base-drive resistor. (DI #2135)

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FIGURE 1



DESIGN EQUATIONS:

$$R_3 = 100k \times (\text{NO. OF CELLS} - 1).$$

$$I_{PEAK} = I_{AVERAGE} + (\Delta I / 2).$$

$$R_5 = V_{HYSTERESIS} / \Delta I = 48 \text{ mV} / \Delta I.$$

$$L_1 = [(V_{OUT} + V_{DIODE})(V_{IN} - V_{OUT})] / (V_{IN} + V_{DIODE})(F).$$

$$R_8 = [100 \text{ mV} + (I_{PEAK} \times R_3)] / 30 \mu\text{A}.$$

$$R_6 = (R_7 \times R_{NTC} \text{ AT } T_{MAX}) / (R_7 + R_{NTC} \text{ AT } T_{MAX}).$$

$$R_9 = (V_{IN} - V_{OUT} - V_{LED}) / I_{TRICKLE}.$$

$$R_{NTC} \text{ AT } T_{MAX} = 4.6 \text{ k}\Omega.$$

$$F_{MIN} > 20 \text{ kHz}.$$

$$I_{AVERAGE} = \text{BATTERY-CHARGE CURRENT}.$$

$$\Delta I = \text{ALLOWABLE VARIATION IN CHARGE CURRENT}.$$

A fast-charge controller IC and surrounding circuitry precisely regulate the charging current, as well as implement peak-voltage fast-charge termination with maximum-temperature backup shutdown.

Capacitor model accounts for temperature, bias

DEBRA HORVITZ, GALAHAD SYSTEMS, LAGUNA HILLS, CA

The basic passive components in Spice are all ideal elements that include no parasitics, such as capacitor ESR and inductor series resistance. Although it is common to represent a real capacitor with a combination of ESR, equivalent series inductance (ESL), and nominal capacitance (C), a more realistic subcircuit representation of a ceramic capacitor takes many more capacitor characteristics into account (Figure 1a).

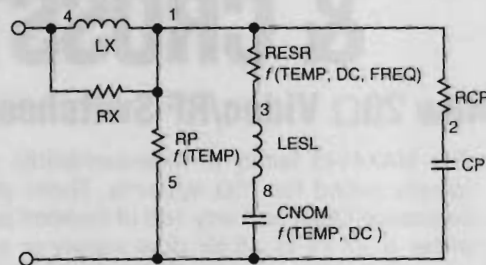
This model features an ESR value, RESR, that depends on frequency, dc bias, and temperature. The capacitance, CNOM, depends on dc bias and temperature. The parallel resistor, RP, which represents the leakage or insulation resistance, is also temperature-dependent. RCP and CP create a secondary and parallel resonance that represents a capacitance that shunts the RLC elements. CP depends on the body and chip size. LX keeps the parallel resonance in check and accounts for pad and lead inductances.

The netlist of the .SUBCKT model (Figure 1b) incorporates a number of equations for various capacitor characteristics (Figure 1c). For example, the definition of RESR in Figure 1b includes Rnom, which is the minimum resistance at the self-resonance frequency. The "Fres" variable determines this frequency. The 1.5 factor in the frequency term widens the self resonance; that is, produces a wider frequency response around the resonance frequency. A value of 1.5 produces the best fit to actual data.

The model incorporates frequency dependence by including the "Freq" term in the resistance expression. During an ac analysis, Spice sets the Freq term to the simulation frequency. During a transient analysis, Freq is equal to 0, which makes the ESR large. The "R=" part is necessary only when Spice re-evaluates the resistance during the simulation. Spice automatically evaluates the expressions and variables in braces, {}, before running the simulation.

Note that in IsSpice4 (Intusoft, San Pedro, CA), the version of Spice this model uses, you can also use a ratio of Laplace polynomial expressions. These Laplace blocks have

FIGURE 1



(a)

```
.SUBCKT CX7R 4 5 ; X7R Ceramic capacitor model
RP 1 5 {1000/Cnom} * {5^((25-TTest)/100)}
RESR 1 3 R = {Rnom} * {5^((25-TTest)/100)} *
+ (1+10^((Abs(Log((Fres)/(Freq+1u)))-1.5) * {(1-(Vbias*0.2/Vnom))} ))
CNOM 6 5 {Cnom} * (1-(Vbias*0.2/Vnom)) * 1-(((TTest-30)/85)^2) * .12))
* C = Cnom * Bias term * Temperature term
RCP 1 2 {1000 * Rnom} ; typical parallel resonant RC, 3 1000 * Rnom
CP 2 5 1p ; set to achieve secondary parallel resonance
LESL 3 6 2nH ; typical effective series inductance
LX 4 1 .1nH ; typical external inductance
RX 4 1 150 ; RX+RCP should approach impedance of free space, 377 ohms).
.ENDS
```

(b)

SELF-RESONANCE FREQUENCY: $Fres = 1/(2\pi\sqrt{ESL \cdot Cnom})$
 ESR/CAP DC-BIAS VARIATION: $nom \cdot (1 - (Vtest/Vnom)^{0.2})$
 ESR(Rnom) FREQUENCY VARIATION: $Rnom \cdot (1 + 10^{((\log(Fres/Freq) - 1.5))})$
 ESR TEMPERATURE VARIATION: $Rnom \cdot 5^{((25 - Ttest)/100)}$
 C TEMPERATURE VARIATION: $Cnom \cdot (1 - ((Ttest - 30)/85)^{2 \cdot 0.12})$

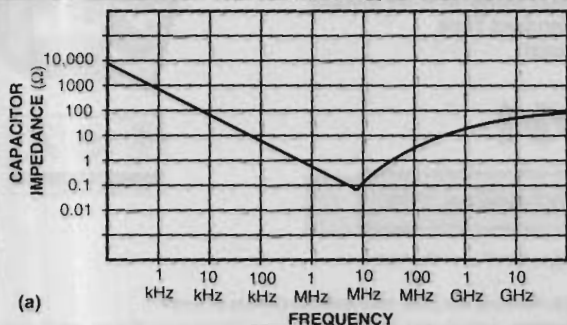
(c)

A complete Spice capacitor model (a) includes elements that depends on frequency, dc bias, and temperature. The corresponding .SUBCKT listing (b) incorporates various equations (c) that govern the model's operation.

both an ac and a transient response and are useful for deriving virtually any linear transfer function of s.

TTest is the temperature of the capacitor, which you can set using the keyword TEMP (using a " = .Options Temp value" statement) in the main Spice netlist. Vbias is the dc bias of the capacitor. Vnom is the voltage at which the capacitance drops by 20%.

FIGURE 2



(a)

(b)

```
.SUBCKT CX7R1206 4 5 ; X7R 1206 0.22uF ceramic capacitor model
RP 1 5 R = 4.5455G * {5^((25-TTest)/100)}
RESR 1 3 R = .067 * {5^((25-TTest)/100)} *
+ (1+10^((Abs(Log(6.38MEG/(Freq+1u)))-1.5) * {(1-(Vbias*0.2/30))} ))
CNOM 6 5 C = .1u * {(1-(Vbias*0.2/30))} * {1-(((TTest-30)/85)^2) * .12))
RCP 1 2 67.0
CP 2 5 8.4p
LESL 3 6 2.83nH
LX 4 1 .1nH
.ENDS
```

The simulation of a 0.22-μF ceramic capacitor shows the impedance variation with frequency (a). In the corresponding .SUBCKT listing (b), the Fres variable is 6.38 MHz and Vnom is 30.

Figure 2a and the corresponding netlist (**Figure 2b**) show the simulation of a 0.22- μ F ceramic capacitor (X7R 1206) with a Fres variable of 6.38 MHz and a Vnom of 30. **Reference 1** provides further derivation of and reasoning behind the equations in **Figure 2**. It also provides equations for NP0, COG, and Y5V capacitor families. You can download the listings for this idea from EDN's Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2119. (DI #2119)

Reference

1. Prymak, John, "Spice modeling of capacitors," CARTS 95: 15th Capacitor and Resistor Technology Symposium, March 1995.

To Vote For This Design, Circle No. 513

Pulsed sensor extends battery life

TERRY MILLWARD, MAXIM INTEGRATED PRODUCTS, READING, UK

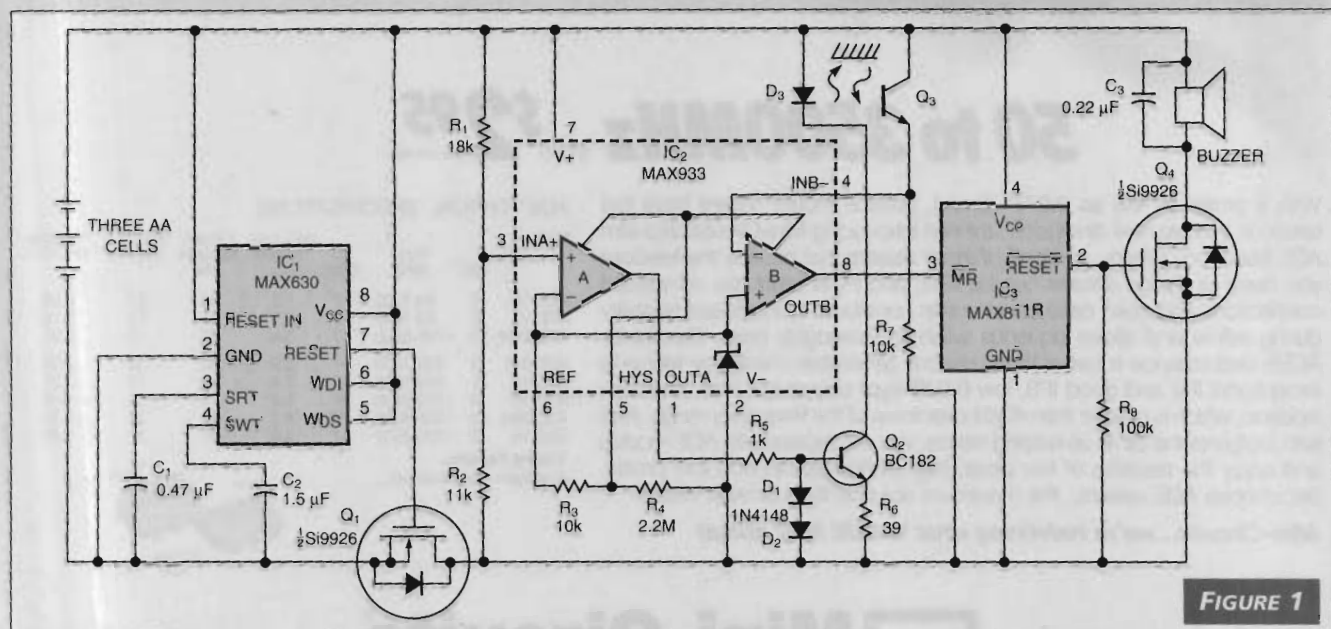
Activating the sensor circuit in **Figure 1** for 1 sec every 30 minutes lowers its 20-mA supply current to an average of 70 μ A. For a battery comprising three AA Duracells, this pulsed operation extends the battery's life to several years. The sensor uses an optocoupler and an IR-emitting diode. Designed to monitor the level of salt crystals in a water softener, the sensor relies on a reflection from the crystals to generate a "no-alarm" level of emitter current in the Q_3 phototransistor. As the salt level drops past the sensor's position, this current level makes a step-change downward.

When the drop across R_7 equals the reference voltage in the comparator/reference device, IC_{2B} , comparator IC_{2B} 's output switches high and releases the manual reset on the voltage monitor, IC_3 . After a minimum reset-delay interval of 140 msec, Q_4 turns on and sounds the buzzer. Comparator IC_{2A} monitors the battery voltage via R_1 and R_2 ; for levels above 3V, the comparator activates the IR-emitting diode, D_3 , by turning on the constant-current sink comprising Q_2 and associated components. Thus, the buzzer sounds for 1

sec every 30 minutes if the battery voltage is below 3V or if the salt level is low.

Power for the sensor is available only when Q_1 turns on. IC₁, a μP supervisor configured as a timebase generator, controls Q_1 . IC₁ consumes less power and has a smaller footprint than the alternative 5556 timer or a 555 timer with multi-stage counters. IC₁ also eliminates the large capacitors otherwise required. Connected directly across the battery, IC₁ draws 60 μA at 3V. IC₁'s external connections cause its internal watchdog timer to cycle repeatedly. With $C_2=1.5 \mu F$, the internal time-out is 3.6 sec; connecting WDS high multiplies this value by 500, extending it to 30 minutes. Each time-out produces a reset pulse that applies power to the remaining circuitry by turning on Q_1 for approximately 1 sec. From IC₁'s data sheet, $t_{RESET}=2.67C_1=1.25$ sec, and $t_{WATCHDOG}=2.67C_2 \times 500=30$ minutes. (DI #2139)

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**FIGURE 1**

Powered by three AA cells, this optoelectronic sensor has a battery life of several years.